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Dated: August 9, 2006 Signature: Valerie Cohen
(Valerie Cohen)

Docket No.: 524322001200
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Eitan CADOURI

Application No.: 10/799,061 Art Unit: 2829

Filed: March 12, 2004 Examiner: J. Hollington

For: SELECTING DIE PLACEMENT ON A SEMICONDUCTOR WAFER TO REDUCE TEST TIME

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

A Notice of Appeal was filed on May 9, 2006. The fees required under § 41.20(b)(2) are dealt with in the accompanying Fee Transmittal.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal
VII.	Argument
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I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

PDF Solutions, Inc., a California corporation, with a principal place of business in San Jose, California.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 16 claims pending in the present application.

B. Current Status of Claims

1. Claims canceled: 0
2. Claims withdrawn from consideration but not canceled: 0
3. Claims pending: 1-16
4. Claims allowed: 0
5. Claims rejected: 1-16

C. Claims on Appeal

The claims on appeal are claims 1-16.

IV. STATUS OF AMENDMENTS

Applicant filed an Amendment after Final Rejection on March 9, 2006. An Advisory Action was mailed on March 28, 2006, indicating that the Amendment did not place the application in a condition for allowance.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 1, 8, and 14 recite methods and a system to select a die placement of dies on a wafer to reduce test time of the dies. (Page 1, paragraph [0001]; page 2, paragraph [0012], lines 1-2.) A die placement is obtained. (Page 2, paragraph [0012], lines 2-5; FIG. 1, 102; FIG. 2-A, 202.) The obtained die placement defines the locations on the wafer on which the dies are to be fabricated. (Page 1, paragraph [0003]; FIG. 2-A, 202.) Placements of a tester head needed to test the dies in the die placement are determined. (Page 3, paragraphs [0013]-[0019]; FIG. 1, 104; FIGs. 2-A, 3-A to 3-E.) A number of touchdowns needed in the determined placements of the tester head is determined. (Page 4, paragraph [0020]; FIG. 1, 106; FIGs. 2-A, 3-A.) A touchdown involves lowering the tester head to form an electrical contact between pins on the tester head and bonding pads on a die being tested. (Page 3, paragraph [0015]; FIG. 3-B.) The die placement is adjusted to reduce the number of touchdowns. (Page 4, paragraph [0021]; FIG. 1, 108; FIG. 2-A.)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1 and 2 are indefinite under 35 U.S.C. 112, second paragraph.

The Examiner objected to claims 1 and 2 based on an informality, presumably on the basis that the Applicant had made a typographical error. Applicant's use of the indefinite article in these claims, however, is not a typographical error. Thus, Applicant believes that the proper statutory basis for the Examiner's objection to these claims is under 35 U.S.C. 112, second paragraph.

B. Whether claims 1-16 are unpatentable under 35 U.S.C. 103(a) over U.S. Patent No. 6,640,423 (the Johnson reference) in view of admitted prior art.

VII. ARGUMENT

In the Advisory Action, the Examiner maintained the objections to claims 1 and 2. As noted above, although the Examiner has objected to these claims based on informalities, Applicant believes that the proper statutory basis for the Examiner's objection is 35 U.S.C. 112, second paragraph. The Examiner also maintained the rejections of claims 1-16 as being unpatentable. Applicant requests reversal in view of the following remarks.

A. Claim Objections

Applicant asserts that the Examiner is objecting to claims 1 and 2 based on an improper application of a mechanical requirement that an element that is recited with an indefinite article must be following by a definite article. MPEP 2173.02, however, clearly states that the standard for determining whether a claim is definite is, "whether the claim meets the threshold requirements of clarity and precision." Applicant asserts that claims 1 and 2 are clear and precise, and the Examiner's suggested amendments are illogical.

1. Claim 1

The Examiner objected to the use of "a die placement" in both the preamble and step a) of claim 1. The preamble recites that claim 1 is "a method of selecting a die placement." Step a) recites, "obtaining a die placement." The Examiner suggests changing step a) to recite "obtaining the die placement." Applicant asserts, however, that doing so is illogical.

In particular, the preamble recites the purpose of the claim (i.e., to select a die placement). Thus, the purpose of performing steps a)-d) of claim 1 is to **select a die placement**. It is, therefore, illogical for the first step of claim 1 (i.e., step a) to be to **obtain the die placement**. If the die placement, which is to be selected by performing steps a)-d), is obtained in step a), then there would be no purpose to performing steps b)-d). The Examiner has yet to explain why changing step a) to recite "obtaining the die placement" is not illogical in view of Applicant's assertions.

2. Claim 2

The Examiner objected to the use of "a die placement" in claim 2. Note, claim 2 recites iterating steps b) and d) of claim 1. Thus, step d) of "adjusting the die placement" is iterated, which results in multiple die placements being created. Claim 2 recites that steps b) and d) are iterated "to obtain a die placement with a minimum number of touchdowns." Note that the "die placement with a minimum number of touchdowns" may not exist until steps b) and d) are iterated. Thus, using the indefinite article is grammatically and logically appropriate and clear.

B. Claim Rejections – 35 USC 103

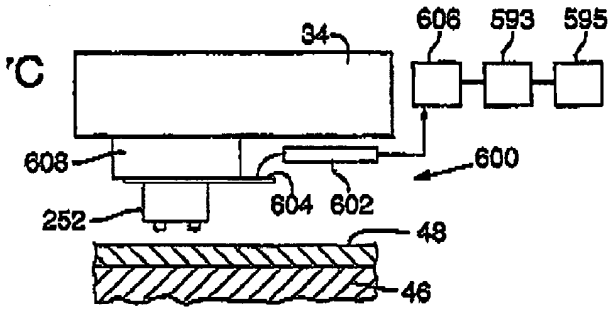
Claims 1-16 stand rejected under 35 USC 103(a) as being unpatentable over US Patent No. 6,640,423 (the Johnson reference) in view of admitted prior art.

Independent claims 1, 8, and 14 recite that the "die placement defines the locations on the wafer on which the dies are to be fabricated." In contrast, the Johnson reference relates to placement and bonding of a die on a substrate **after the die has been diced or cut from the wafer** on which it was formed. Thus, the "die placement" recited in claims 1, 8, and 14 is not the same as the placement of dies referred to in the Johnson reference.

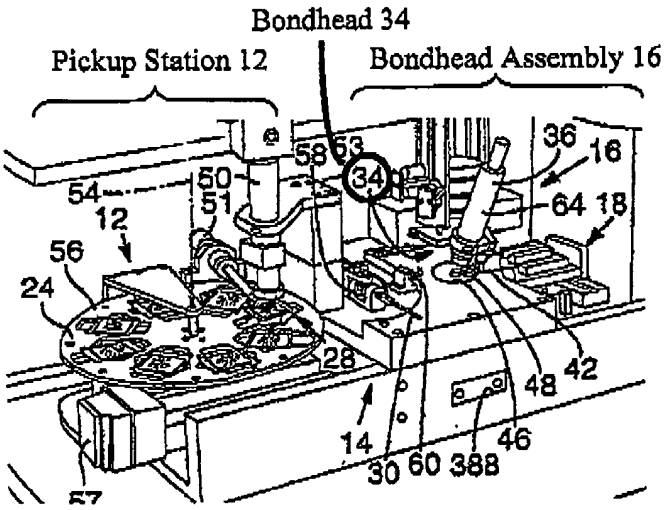
1. Johnson Reference Discloses Testing a Die that has been Cut from the Wafer

In the Advisory Action, the Examiner maintained the rejection of claims 1, 8, and 14, because "after reviewing the Johnson reference, the examiner is unable to locate where it states or even suggest that the testing are done **after the dies have been cut**." (Emphasis added.) The Examiner further states, "[t]he examiner believes that the Johnson reference does test while the **dies are on the wafer**." Applicant asserts that the Examiner's reading of the Johnson reference is contradicted by clear and explicit disclosure in the Johnson reference.

The Examiner has asserted that probe 604 disclosed in the Johnson reference corresponds to the probe head recited in claim 1. As clearly shown in FIG. 47C (reproduced below) and described in column 33, lines 63-67, probe 604 is mounted on bondhead 34.



As clearly shown in FIG. 2 (reproduced below) and described in column 6, lines 56-58, bondhead 34 is located on bondhead assembly 16.



As also shown in FIG. 2 above and described in column 6, lines 49-52, a transfer arm 30 "moves between pickup station 12 and bondhead assembly 16 to transfer die 26 therebetween." Column 8, lines 1-10, disclose that rotating carrier 56 in pickup station 12 includes eight recesses that support eight die holders.

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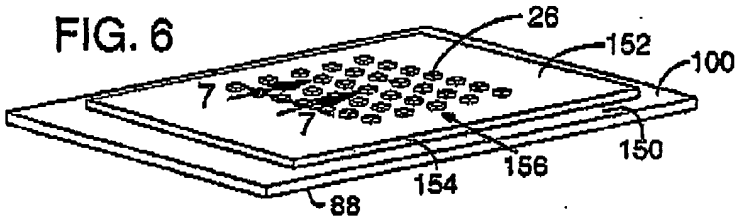
As shown in FIG. 6 (reproduced below) and described in column 10, lines 49-51, multiple dice 26 are supported on a die holder 100:

FIG. 6



As can be clearly seen in FIG. 6 above, the dies on die holder 100 are individual dies that have already been cut from a wafer. Thus, in the Johnson reference, transfer arm 30 transfers an individual die from die holder 100 in pickup station 12 to bondhead assembly 16. In bondhead assembly 16, the individual die is bonded to substrate 48 using bondhead 34.

Thus, the explicit disclosure of the Johnson reference contradicts the Examiner's assertion that the dies in the Johnson reference are not cut from the wafer and that they are tested while still on the wafer. In particular, FIG. 6 clearly shows the dies as being individual dies and not as dies formed on a wafer. As described above, an individual die is transferred to be tested by probe 604 and bonded to substrate 48 in bondhead assembly 16 rather than dies on a wafer.

Additionally, the Johnson reference discloses in column 8, lines 32-33, "a 'die' can be anything that can be picked, placed, and then bonded in a desired location." Applicant asserts that it is not possible to pick, place, and bond a die that is still on a wafer. Instead, only a die that has already been cut from the wafer can be "picked, placed, and then bonded in a desired location."

Furthermore, the Johnson reference discloses in the TECHNICAL FIELD section in column 1, lines 6-8, "[t]he present invention relates to an improved apparatus and method for the placement and flipchip bonding of a die on a substrate..." It is well known in the art that a die is bonded on a substrate only after the die has been cut from the wafer. Dies that are still on the wafer are not bonded.

Thus, Applicant asserts that the Johnson reference clearly discloses placement of a die after the die has been cut from a wafer rather than a die placement of dies to be formed on a wafer.

2. Johnson Reference Fails to Disclose Adjusting Die Placement to Reduce Number of Touchdowns by Probe

As noted above, the Examiner has asserted that probe 604 disclosed in the Johnson reference corresponds to the tester head recited in claim 1. Claims 1, 8, and 14 recite that the die placement is adjusted to reduce the number of touchdowns (the number of times the tester head is lowered) to test the dies in the die placement. However, as depicted in FIG. 47C and described in column 33, lines 50-67, probe 604 is a component of an oscillation frequency detection assembly 600 that controls the amount of bump height compression of the die, the substrate, or both, during bonding. The Johnson reference does not disclose adjusting the die placement on die holder 100, located in pickup station 12, to reduce the number of touchdowns by probe 604, located in bondhead assembly 16.

3. No Motivation to Combine Johnson Reference and Admitted Prior Art

The Examiner has agreed that the Johnson reference does not disclose die placements that "define the locations on the wafer as claimed." The Examiner, however, asserts that, "the admitted prior art discloses that it is well known to use the die placement to define the location on the wafer, which the dies are to be fabricated." The Examiner cites to page 1, paragraphs [0003] and [0004] of the present specification. The Examiner also asserts that "[i]t would have been well known and obvious to a person having ordinary skill in the art at the time the invention was made to have the die placement in Johnson et al. to define the location on the wafer since the prior art teaches that having the die placement to define the location on the wafer helps track the locations of the dies that fail or have low yield during test." Applicant asserts that the Examiner's assertion is illogical, and that there is no motivation to combine the Johnson reference and admitted prior art.

In particular, as discussed above, the placement of dies referred to in the Johnson reference are of dies **after they have been cut from the wafer**. In contrast, the testing referred to in paragraph [0004] of the present specification refers specifically to testing the dies **while the dies**

are still on the wafer. Specifically, lines 3-4 of paragraph [0004] states, "[s]emiconductor manufacturers are increasingly performing comprehensive testing of dies, meaning that each die is tested, **while the dies are still on the wafer**." (Emphasis added.) Thus, the testing described in paragraph [0004] is incompatible with the testing disclosed in the Johnson reference because paragraph [0004] describes **testing dies that are still on the wafer** while the Johnson reference discloses **testing dies after they have been cut from the wafer**.

MPEP 2143.01(VI) states, "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." In the present case, the Johnson reference discloses testing a die that has been cut from the wafer, while paragraphs [003] and [0004] of the present specification relates to testing dies that are still on the wafer. Thus, the Examiner's proposed combination would require changing the principle of operation of either the Johnson reference or what is disclosed in paragraphs [0003] and [0004]. Applicant, therefore, asserts that the Examiner has failed to establish a prima facie case of obviousness.

For at least the reasons set forth above, Applicant asserts that claims 1, 8, and 14 are allowable over the Johnson reference. Additionally, Applicant asserts that claims 2-7, 9-13, and 15, 16 are allowable for at least the reason that they depend from allowable independent claims. Thus, Applicant requests reversal of the Examiner's rejection of claims 1-16.

VIII. CLAIMS APPENDIX

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE APPENDIX

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS APPENDIX

None.

In view of the above, Applicant request reconsideration and reversal of the rejection of pending claims 1-16.

Dated: August 9, 2006

Respectfully submitted,

By _____

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APPENDIX A

Claim 1 (Previously Presented): A method of selecting a die placement of dies on a wafer to reduce test time of the dies, the method comprising:

a) obtaining a die placement of dies on the wafer, wherein the die placement defines the locations on the wafer on which the dies are to be fabricated;

b) determining placements of a tester head needed to test the dies in the die placement;

c) determining a number of touchdowns needed in the determined placements of the tester head, wherein a touchdown involves lowering the tester head to form an electrical contact between pins on the tester head and bonding pads on a die being tested; and

d) adjusting the die placement to reduce the number of touchdowns.

Claim 2 (Original): The method of claim 1, wherein steps b) to d) are iterated to obtain a die placement with a minimum number of touchdowns needed to test the dies in the die placement.

Claim 3 (Original): The method of claim 1, wherein the placements of the tester head are determined based on a test program.

Claim 4 (Original): The method of claim 3, wherein steps a) to d) are iterated for different test programs to determine a combination of die placement and test program with a minimum number of touchdowns.

Claim 5 (Original): The method of claim 4, wherein steps a) to d) are iterated for different tester heads to determine a combination of die placement, test program, and tester head with a minimum number of touchdowns.

Claim 6 (Original): The method of claim 1, wherein steps a) to d) are iterated for different tester heads to determine a combination of die placement and tester head with a minimum number of touchdowns.

Claim 7 (Original): The method of claim 1, wherein the tester head is configured to simultaneously test a set of multiple dies.

Claim 8 (Previously Presented): A method of selecting a die placement of dies on a wafer to reduce test time of the dies, the method comprising:

a) obtaining a die placement of dies on the wafer, wherein the die placement defines the locations on the wafer on which the dies are to be fabricated;

b) obtaining a configuration of a tester head used to test the dies on the wafer;

c) determining placements of the tester head needed to test the dies in the die placement using the configuration of the tester head;

d) determining a number of touchdowns needed in the determined placements of the tester head; and

e) adjusting the die placement to reduce the number of touchdowns.

Claim 9 (Original): The method of claim 8, wherein steps c) to e) are iterated to obtain a die placement with a minimum number of touchdowns needed to test the dies in the die placement.

Claim 10 (Original): The method of claim 8, wherein the placements of the tester head are determined based on a test program.

Claim 11 (Original): The method of claim 10, wherein steps a) to e) are iterated for different test programs of tester heads to determine a combination of die placement and test program with a minimum number of touchdowns.

Claim 12 (Original): The method of claim 11, wherein steps a) to e) are iterated for different configurations of tester heads to determine a combination of die placement, test program, and configuration of tester head with a minimum number of touchdowns.

Claim 13 (Original): The method of claim 8, wherein steps a) to e) are iterated for different configuration of tester heads to determine a combination of die placement and configuration of tester head with a minimum number of touchdowns.

Claim 14 (Previously Presented): A system of selecting a die placement of dies on a wafer to reduce test time of the dies, the system comprising:

an initial die placement of dies on the wafer, wherein the initial die placement defines the locations on the wafer on which the dies are to be fabricated;

a tester head having pins to contact bonding pads on a die on the wafer being tested; and

an adjusted die placement, wherein the adjusted die placement is derived from the initial die placement by determining placements of the tester head needed to test the dies on the initial die placement and a number of touchdowns needed in the determined placements of the tester head, and wherein the adjusted die placement requires fewer touchdowns by the tester head to test the dies on the adjusted die placement than the dies on the initial die placement.

Claim 15 (Original): The system of claim 14, wherein the initial die placement and the adjusted die placement have the same number of dies.

Claim 16 (Original): The system of claim 14, wherein the tester head is configured to simultaneously test a set of multiples dies.